

Ingress

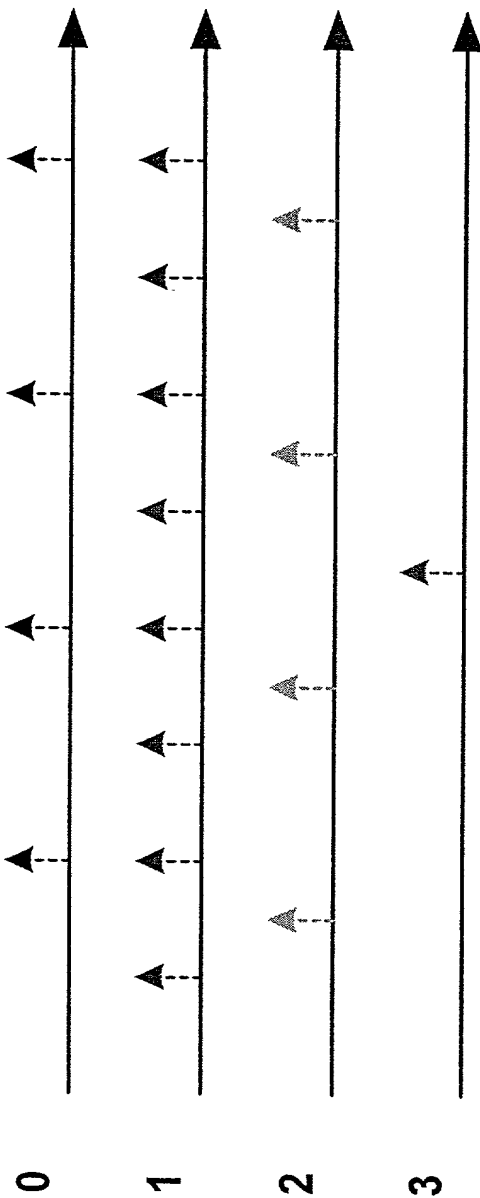


Fig. 1a

Multicast Schedule

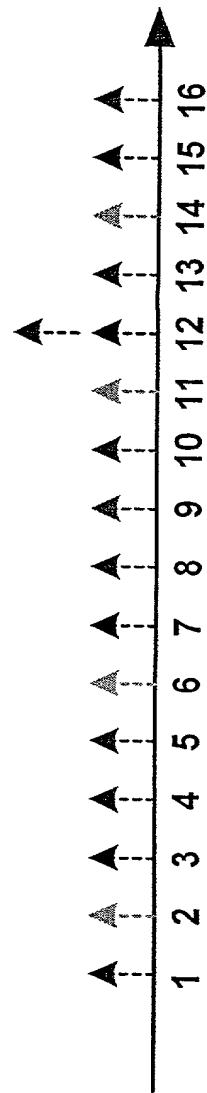


Fig. 1b

Fig. 2a

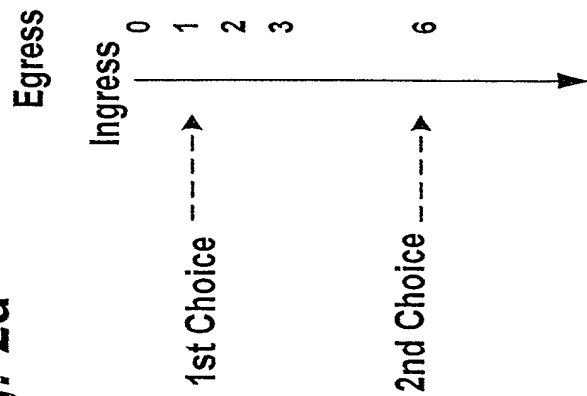


Fig. 2c

Multicast Cell Fanout Table

				Egress														
				0	1	2	3	Ingress										
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	0	1	1	1	0	0	0	0	1	1	0	1	1	0	1	1	0	1
0	1	1	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1
0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	0
0	0	0	0	0	1	1	0	0	1	1	0	1	1	0	1	1	0	1

Fig. 2d

Eligible											Compile Control Frame										
1	1	1	1	1	1	1	0				1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	0				1	1	1	1	1	1	1	1	1	1	1

Fig. 2e

Multicast Egress Credit

27	0	35	5
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Fig. 2b

Fig. 2